Amendments to the Written Description of the Specification

Applicant presents replacement paragraphs below indicating the changes with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing.

On page 1, after the title insert: --Background Of The Invention--;

On page 1, after "Background of the Invention" but before the first paragraph insert --1. Field of the Invention--;

On page 1, before the second paragraph beginning on line 10, insert --2. Discussion of the Related Art--;

Please amend the second paragraph on page 1 as shown below:

--Fig. 1 shows an SRAM cell circuit with six transistors. The cell ~~comprises~~ includes a memory point formed of two inverters I1 and I2 connected head-to-tail and having their two inputs, respectively BLTI, BLFI, connected to bit lines BLT, BLF by N-channel MOS transistors (NMOS) T1, T2. The gates of transistors T1 and T2 are connected to a word line WL. Inverter I1 comprises a PMOS transistor TP1 and an NMOS transistor TN1. The gates of transistors TP1 and TN1 are connected to terminal BLTI of the inverter. The drains of transistors TP1 and TN1 are connected and form the output terminal of the inverter. The sources of transistors TP1 and TN1 are respectively connected to a supply voltage VDD and a ground GND. Inverter I2 has the same structure and includes a PMOS transistor TP2 and an NMOS transistor TN2.—

Please amend the paragraph beginning on page 1, line 17 through page 2, line 6 as shown below:

--Fig. 2 shows a simplified top view of an embodiment in CMOS technology of the SRAM cell of Fig. 1. For simplicity, the P- and N-channel transistors are shown with the same gate widths. N-channel transistors T1, T2, TN1, and TN2 are formed in a P-type substrate (SUB) and P-channel transistors TP1 and TP2 are formed in an N-type well (NWELL). The drain regions of transistors TN1, T1, and TN2, T2 are confounded. The transistor gates, formed of polysilicon, are shown in hatchings. The gates of transistors TP1, TN1, respectively TP2, TN2,

are interconnected. The drains of transistors TP1 and TN1 are connected to the gates of transistors TP2, TN2 by a conductive line formed in an upper metal layer (METAL1) via vias or contacts (the locations of which are shown with crosses). The drains of transistors TP2 and TN2 are connected to the gate of transistors TP1, TN1 by a conductive line formed in the same metal layer (METAL1). Vias form the contact between the source regions of transistors T1, T2, TN1, TN2, TP1, TP2 and metal lines, not shown, respectively connected to lines BLT, BLF and to voltages GND, GND, VDD, and VDD. The N-type well is grounded and the substrate is at a predetermined voltage. For clarity, the STI transistor insulation trenches have not been shown. The STI trenches are preferably the inverse of the active areas (drains or sources).--

On page 2, before line 24, insert --<u>Summary of the Invention</u>--;

Please amend the first two paragraphs on page 3, lines 1-5 as shown below:

--~~A more specific~~ <u>Another</u> object of the present invention is to provide such a structure enabling association of capacitors with an SRAM cell without increasing the surface area of said cell.

~~An~~ <u>Another</u> object of the present invention is to provide a method for manufacturing such a capacitor.--

On page 5, before line 3, insert --<u>Brief Description of the Drawings</u>--;
On page 5, before line 20, insert --<u>Detailed Description</u>--;

Please amend the second paragraph on page 7 as shown below:

--Fig. 4 shows a simplified top view of an SRAM CMOS cell with six transistors associated with capacitors according to the present invention. The SRAM cell comprises two inverters I1 and I2 and two transistors T1, T2 having the same connections and the same dimensions as in Fig. 2. According to a preferred embodiment of the present invention, a same coated region BR1 is arranged so that the drain regions of transistors TP1 and TN1 of inverter I1 each directly rest on a portion of coated region BR1. Further, a projection of the etched polysilicon region forming the gates of transistors TP1 and TN1 is formed to electrically connect

said gates to region BR1 via a contact opening V1. Opening V1 is made between transistors TP1 and TN1 above the border between well NWELL and substrate SUB. As illustrated hereafter in relation with Fig. 5, four capacitors are formed around coated region BR1 connected to the gates of transistors TP1 and TN1 of inverter I1. Similarly, the drain regions of transistors TP2 and TN2 of inverter I2 each directly rest on a coated region BR2 connected by an opening V2 to the gates of transistors TP2 and TN2, and four capacitors are formed around coated region BR2 connected to the gates of transistors TP2 and TN2 of inverter I2. The eight capacitors connected to the gates of the transistors of inverters I1 and I2 ~~enable increasing~~ increases the resistance of the SRAM cell against ionizing radiations.--

Please amend the last paragraph on page 12 as shown below:

--The present invention will also be easily adapted to one or several capacitors coupling other active regions belonging to other types of components of an integrated circuit directly resting on the coated region. The present invention will be especially ~~be~~ easily adapted to capacitors coupling several active regions of several components, each of which directly rests on a portion of the same buried region. The present invention will also easily adapt to a bipolar technology.--

On page 12, line 22 please insert:

--Such alterations, modifications, and improvements are intended to be part of this disclosure, and are intended to be within the spirit and the scope of the present invention. Accordingly, the foregoing description is by way of example only and is not intended to be limiting. The present invention is limited only as defined in the following claims and the equivalents thereto.

What is claimed is:--